PATENT
ATTORNEY DOCKET NO.: 041993-515

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
BOX PATENT APPLICATION
Washington, D.C. 20231

TRANSMITTAL FOR A NEWLY EXECUTED ORIGINAL APPLICATION UNDER 37 C.F.R. §1.53(b)

This is a request for filing a patent application under 37 C.F.R. §1.53(b) for:

Inventors: Seong-Kweon HA and Jong-Hun KIM

For: SEMICONDUCTOR PACKAGE AND FABRICATION METHOD THEREOF

1. This is a new [X] **Utility** [ ] **Design** [ ] **Plant** patent application.

2. The papers enclosed to obtain a filing date are as follows:
   17 Pages of Specification including
   1 Title Page
   5 Pages of Claims
   1 Page of Abstract
   4 Sheets of drawings containing 23 Figures
   [ ] The enclosed drawing(s) are photograph(s), and there is also attached a PETITION TO ACCEPT PHOTOGRAPH(S) AS DRAWING(S)

3. Combined Declaration and Power of Attorney
   [X] Enclosed and is executed by all inventors.
   [ ] Not Enclosed.
   This application is being filed under the provisions of 37 C.F.R. §1.53(f). Applicant(s) await notification from the Patent and Trademark Office of the time set for filing the Declaration and paying the filing fees.

4. Language
   [X] English
   [ ] Non-English
   This application is being filed in accordance with 37 C.F.R. §1.52(d) and §608.01 of the MPEP. Applicant(s) await notification from the Patent and Trademark Office of the time set for filing the verified English translation and the processing fee.

5. Assignment

   [X] An assignment of the invention to Hyundai Electronics Industries Co., Ltd. and a PTO Form-1595, Recordation Form Cover Sheet, are enclosed.

   [ ] An assignment will be filed at a later date.

6. Priority - foreign applications under 35 U.S.C. §119(a)-(d) or §365(b) or PCT international applications under 35 U.S.C. §365(a) designating at least one country other than the U.S.

   [X] Priority of the following foreign application is claimed:

Country	Application No.	Filed
Korea	285/2000	January 5, 2000

   Certified copy: [X] is attached. [ ] will follow.

7. Priority based on provisional application(s) - 35 U.S.C. §119(e)

   [ ] Priority of the following provisional application(s) is claimed:

Application No.	Filed

A. Relate Back - 35 U.S.C. §119(e)

[ ] Amend the specification by inserting before the first line the sentence: "This application claims priority of copending provisional application(s) No. _____ filed on _____."

8. Small entity status

[ ] A statement claiming small entity status under 37 C.F.R. §§1.9 and 1.27 is enclosed.

9. Fee Calculation (37 C.F.R. §1.16)

CLAIMS FOR FEE CALCULATION				
	Number Filed	Number Extra	at Rate of	Basic Fee Utility $710.00 Design $320.00
Total Claims (37 C.F.R. §1.16(c))	20 - 20 =	0	$ 18.00 each=	$0.00
Independent Claims (37 C.F.R. §1.16(b))	4 - 3 =	1	$ 80.00 each=	$80.00
Multiple dependent claim(s), if any (37 C.F.R. §1.16(d))			$270.00	+
			SUB-TOTAL =	**$790.00**
			Reduction by 1/2 for filing by a small entity	**- $**
			TOTAL FILING FEE =	**$790.00**

10. Fee Payment

[ ] Not Enclosed. **NO FEE IS BEING PAID BY CHECK OR DEPOSIT ACCOUNT AT THIS TIME.**
This application is being filed under the provisions of 37 C.F.R. §1.53(f). Applicant(s) await notification from the Patent and Trademark Office of the time set for filing the Declaration and paying the filing fees.

[X] Enclosed.

Two checks in the amounts of $ 790.00 and $40.00 representing the basic filing fee of $710.00, additional claim fee of $80.00 and an assignment recording fee of $40.00 are enclosed.

11. [X] **Except** for issue fees payable under 37 C.F.R. §1.18, the Commissioner is hereby authorized by this paper to charge any additional fees during the entire pendency of this application including fees due under 37 C.F.R. §§1.16 and 1.17 which may be required, including any required extension of time fees, or credit any overpayment to Deposit Account 50-0310. This paragraph is intended to be a **CONSTRUCTIVE PETITION FOR EXTENSION OF TIME** in accordance with 37 C.F.R. §1.136(a)(3).

12. Additional papers enclosed:

[ ] Preliminary Amendment
[ ] Information Disclosure Statement
[ ] Form PTO-1449, ___ document included
[ ] Declaration of Biological Deposit
[ ] Submission of "Sequence Listing", computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.

Please accord this application an application number and filing date.

Respectfully submitted,

MORGAN, LEWIS & BOCKIUS LLP

Mary Jane Boswell
Reg No. 33,652 per

William O. Trousdell
Reg. No. 38,637

Dated: November 13, 2000

Customer No. 009629
MORGAN, LEWIS & BOCKIUS LLP
1800 M Street, N.W.
Washington, D.C. 20036
(202) 467-7000

UNITED STATES PATENT APPLICATION

OF

SEONG-KWEON HA

AND

JONG-HUN KIM

FOR

SEMICONDUCTOR PACKAGE AND FABRICATION METHOD THEREOF

This application claims the benefit of Application No. 285/2000, filed in Korea on January 5, 2000, which is hereby incorporated by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor package and a fabrication method thereof, and in particular to an improved semiconductor package which enhances adhesion between a solder and a package body and improves stability and a fabrication method thereof.

Discussion of the Related Art

There is an increasing demand for miniaturization of non-memory products, such as microprocessors and custom semiconductors ASIC. As a result, in order to utilize a plurality of pins, a ball grid array (BGA) arranging a ball-shaped external terminal below a package has become a main semiconductor package.

The BGA takes concepts of a pin grid array (PGA) and a flip chip. Accordingly, a space of a conventional semiconductor package is reduced by approximately 60%, and electrical and thermal execution power is increased by 40%. In case the BGA uses more than 300 pins, it is advantageous in cost as well.

Various chip size package (CSP) techniques have been recently developed to the extent that the semiconductor chip and package are only slightly different in size. The CSP techniques have been rapidly widespread according to the miniaturization, high speed and high integration tendency of the semiconductor, more than the applicants expected.

In addition, a wafer level package technique performing all assembly steps in a wafer state where chips are not cut is acknowledged as the CSP technique for the next generation. A

semiconductor assembly process is generally performed after cutting a wafer into respective chips. Conversely, in the wafer level package technique, a series of assembly steps, such as die bonding, wire bonding and molding are carried out in the wafer state where the chips are connected, and thereafter the chips are cut. Accordingly, the wafer level package technique can reduce an entire packaging cost more than the currently-used CSP techniques.

Figure 1 illustrates a conventional wafer level chip size package (WLCSP). As depicted in Figure 1, a plurality of chip pads 3 are separately formed on an upper surface of a wafer 1. A passivation layer 5 is formed on the upper surface of the wafer 1 so that a region of an upper surface of the plurality of chip pads 3 are exposed. An under bump metallurgy (UBM) 7 is formed at upper surfaces of the plurality of chip pads 3 exposed through the passivation layer 5. The UBM 7 is formed in order to enhance adhesion between the plurality of chip pads 3 and a solder ball 9 (to be discussed later) and generally consists of a 2- to 3-level metal layer. After forming the UBM 7, a solder paste is coated on upper surfaces of the UBM 7 and the passivation layer 5. The solder ball 9 is formed after a reflow step, thereby fabricating the WLCSP.

One disadvantage of the conventional WLCSP is that adhesion between the solder ball 9 and the UBM 7 is weak. Accordingly, separation may take place due to the weak adhesion between the solder ball 9 and the UBM 7, after constant switching operations of a chip. Therefore, the solder ball 9 may be easily separated from a package body. Another disadvantage of the conventional WLCSP is that materials constituting the UBM 7 are difficult to combine.

SUMMARY OF THE INVENTION

Accordingly, the present invention is directed to a semiconductor package and a method of fabricating the same that substantially obviates one or more of the problems due to the limitations and disadvantages of the related art.

An object of the present invention to prevent a solder ball from being separated from a semiconductor package.

It is another object of the present invention to improve performance and reliability of a package, when constituting a metal layer in a wafer level chip size package.

Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, the semiconductor package includes a semiconductor substrate; a plurality of chip pads separately formed on an upper surface of the semiconductor substrate; an irregular metal pattern being electrically connected to the plurality of chip pads; and an external terminal electrically connected to the metal pattern.

In another aspect of the present invention, the semiconductor package includes a semiconductor substrate; a plurality of chip pads being separately formed on an upper surface of the semiconductor substrate; a first metal pattern formed on upper surfaces of the plurality of

chip pads; a second metal pattern having an irregular shape, and formed on an upper surface of the first metal pattern; and an external terminal electrically connected to the second metal pattern.

In a further aspect of the present invention, there is provided a method of fabricating the semiconductor package including the steps of separately forming a plurality of chip pads on an upper surface of a semiconductor substrate; forming an irregular metal pattern electrically connected to the plurality of chip pads; and forming an external terminal electrically connected to the metal pattern.

In yet a further aspect of the present invention, there is provided a method of fabricating the semiconductor package including the steps of separately forming a plurality of chip pads on an upper surface of a semiconductor substrate; forming a first metal pattern on upper surfaces of the plurality of chip pads; forming a second metal pattern having an irregular shape on an upper surface of the first metal pattern; and forming an external terminal electrically connected to the second metal pattern.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of the specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

Figure 1 is a cross-sectional view illustrating a conventional wafer level chip size package;

Figure 2 is a cross-sectional view illustrating a wafer level chip size package in accordance with a preferred embodiment of the present invention;

Figures 3A to 3J are cross-sectional views illustrating a method of fabricating the wafer level chip size package in accordance with a preferred embodiment of the present invention; and

Figures 4A to 4K are cross-sectional views illustrating a method of fabricating the wafer level chip size package in accordance with another preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A structure of a semiconductor device and a fabrication method thereof in accordance with a preferred embodiment of the present invention will now be described in detail with reference to the accompanying drawings. Here, a WLCSP is exemplified. However, the present invention may be applied to different kinds of packages.

Figure 2 illustrates a WLCSP 125 in accordance with the preferred embodiment of the present invention. As depicted therein, a plurality of chip pads 103 are separately formed on an upper surface of a semiconductor substrate 100 in a wafer state. A first insulation layer 105, which includes polymide or benzocyclobutene (BCB), is formed on a region of the upper surface of the semiconductor substrate 100 that is not occupied by the plurality of chip pads 103. A first metal pattern 107 is electrically connected to the plurality of chip pads 103 and separately formed on upper surfaces of the plurality of chip pads 103 and the first insulation layer 105. The first metal pattern 107 may include Ti, Al or Cr. The preferred embodiment employs Ti

which has superior adhesion with a polymer, a nitride and an oxide on the semiconductor substrate 100, and has a small contact resistance. A second metal pattern 109 of an irregular shape is formed on a region of the first metal pattern 107. Various metals may be used as a material of the second metal pattern 107. The preferred embodiment employs Ni which has superior adhesion with a solder, and also has small reactivity with the solder. A second insulation layer 113, which mostly includes photoresist or BCB, is formed thick on upper surfaces of the first insulation layer 105 and the first metal pattern 107 in order to seal up the first insulation layer 105, the first metal pattern 107 and the second metal pattern 109. At this point, an upper surface and side portions of the second metal pattern 109 are not sealed up. In the preferred embodiment, the second insulation layer 113 may include the photoresist or BCB. A solder mask 115 is formed on an upper surface of the second insulation layer 113 so that the second metal pattern 109 is exposed. The solder mask 115 protects metal wiring and determines a position of a solder ball 111. In case the second insulation layer 113 consists of the BCB, the solder mask 115 may not be provided. The solder ball 111 is electrically connected to the upper surface and the side portions of the second metal pattern 109 and is formed as an external terminal on a surface of the second metal pattern 109 exposed through the solder mask 115.

Figures 3A to 3J are cross-sectional views illustrating a preferred embodiment of a method of fabricating a semiconductor package in accordance with the present invention.

As illustrated in Figure 3A, a semiconductor substrate 100 in a wafer state is prepared. Here, a plurality of chip pads 103 are separately formed on an upper surface of the semiconductor substrate 100.

As shown in Figure 3B, upper surfaces of the semiconductor substrate 100 and the plurality of chip pads 103 are coated with a polymide or BCB, and patterned. Accordingly, a first insulation layer 105 is formed so that the upper surfaces of the plurality of chip pads 103 are exposed.

As depicted in Figure 3C, a metal layer 106, including Ti, is deposited according to a deposition method, such as a sputtering process, on upper surfaces of the first insulation layer 105 and the plurality of exposed chip pads 103.

As illustrated in Figure 3D, a pad redistribution step is performed in order to form a first metal pattern 107, which is electrically connected to the plurality of chip pads 103, by patterning the metal layer 106.

Since a distribution pitch of the plurality of chip pads 103 is only 100 to 150 mm, it is difficult to directly form a solder ball 111 on the plurality of chip pads 103. In addition, when a package is fabricated and mounted on a printed circuit board (PCB), intervals and distribution of the solder ball 111 needs to be adjusted, which is the reason a pad redistribution step is carried out.

As shown in Figure 3E, a photoresist layer 112 is spread thick on upper surfaces of the first metal pattern 107 and the first insulation layer 105.

Thereafter, as illustrated in Figure 3F, a second insulation layer 113 is formed by patterning the photoresist layer 112 in order to form an irregular photoresist layer pattern 114 on a portion of the first metal pattern 107.

As depicted in Figure 3G, a second metal pattern 109, having an irregular shape, is formed by filling nickel in a space of the irregular photoresist layer pattern 114. A step for

filling nickel may be performed according to a deposition method, such as the sputtering process. However, in the present embodiment, an electro-plating process is utilized due to restriction of thickness.

As illustrated in Figure 3H, a solder mask 115 is formed on an upper surface of the second insulation layer 113 so that the second metal pattern 109 and the irregular photoresist layer pattern 114 are exposed. The solder mask 115 prevents solder from being covered at unnecessary portions during a succeeding solder paste covering step and a reflow step.

As depicted in Figure 3I, the irregular photoresist layer pattern 114 exposed through the solder mask 115 is removed.

Thereafter, a solder paste is covered on an upper surface of a package body 120 illustrated in Figure 3I, and the reflow step is carried out thereon. The solder ball 111 is electrically connected to upper and side portions of the exposed second metal pattern 109 and is formed as an external terminal, thereby finishing fabrication of the WLCSP 125.

Figures 4A to 4K are cross-sectional views illustrating another preferred embodiment of a method of fabricating a semiconductor package in accordance with the present invention.

As illustrated in Figure 4A, a semiconductor substrate 100 in a wafer state is prepared. Here, a plurality of chip pads 103 are separately formed on an upper surface of a semiconductor substrate 100.

As shown in Figure 4B, upper surfaces of the semiconductor substrate 100 and the plurality of chip pads 103 are coated with a polymide or BCB, and patterned. Accordingly, a first insulation layer 105 is formed so that upper surfaces of the plurality of chip pads 103 are exposed.

As depicted in Figure 4C, a metal layer 106, including Ti, is deposited according to a deposition method, such as the sputtering process, on upper surfaces of the first insulation layer 105 and the exposed plurality of chip pads 103.

As illustrated in Figure 4D, a pad redistribution step is performed in order to form a first metal pattern 107, which is electrically connected to the plurality of chip pads 103, by patterning the metal layer 106.

As shown in Figure 4E, a photoresist layer 112 is spread thick on upper surfaces of the first metal pattern 107 and the first insulation layer 105.

As illustrated in Figure 4F, the photoresist layer 112 is patterned so that an irregular photoresist layer pattern 114 is formed on a region of the first metal pattern 107.

Thereafter, as depicted in Figure 4G, a second metal pattern 109, having an irregular shape, is formed by filling nickel in a space 114' of the irregular photoresist layer pattern 114 according to an electro-plating process.

As illustrated in Figure 4H, the photoresist layers, including the irregular photoresist layer pattern 114 illustrated in Figure 4G, are removed.

As shown in Figure 4I, a BCB layer 135 is spread thick on an upper surface of the package body 130 shown in Figure 4H, thereby sealing up the second metal pattern 109 having an irregular shape.

As depicted in Figure 4J, a second insulation layer 113 is formed by patterning the BCB layer 135 so that an upper surface and side portions of the second metal pattern 109 are exposed.

As illustrated in Figure 4K, a solder paste is spread on an upper surface of a package body 140 as shown in Figure 4J, and a reflow process is performed thereon. Accordingly, a solder

ball 111, electrically connected to the upper and side portions of the exposed second metal pattern 109, is formed as an external terminal, thereby completing a WLCSP 125 in accordance with another preferred embodiment of the present invention.

As discussed earlier, in a semiconductor package in accordance with the present invention, an adhesion portion of a package body to the solder ball 111 includes a metal having an irregular shape, and thus an adhesion side thereof is increased, thereby improving adhesion strength between the solder ball 111 and the package body. As a result, the solder ball 111 is prevented from separating from the package body, thereby improving reliability of the semiconductor package.

In addition, in the semiconductor package in accordance with the present invention, respective metal layers are formed by different steps. Accordingly, it is easy to respectively select materials of the metal layers.

Moreover, the semiconductor package of the present invention can be fabricated according to a conventional package method by using identical devices as the conventional ones. Therefore, it is easy to apply the present invention.

As the present invention may be embodied in several forms without departing from the spirit or essential characteristics thereof, it should also be understood that the above-described embodiment is not limited by any of the details of the foregoing description, unless otherwise specified, but rather should be construed broadly within its spirit and scope as defined in the appended claims, and therefore all changes and modifications that fall within the meets and bounds of the claims, or equivalents of such meets and bounds are therefore intended to be embraced by the appended claims.

What is claimed is:

1. A semiconductor package comprising:

a semiconductor substrate;

a plurality of chip pads separately formed on an upper surface of the semiconductor substrate;

an irregular metal pattern electrically connected to the plurality of chip pads; and

an external terminal electrically connected to the metal pattern.

2. A semiconductor package comprising:

a semiconductor substrate;

a plurality of chip pads separately formed on an upper surface of the semiconductor substrate;

a first metal pattern formed on upper surfaces of the plurality of chip pads;

a second metal pattern having an irregular shape and formed on an upper surface of the first metal pattern; and

an external terminal electrically connected to the second metal pattern.

3. The semiconductor package according to claim 2, wherein the first metal pattern includes titanium.

4. The semiconductor package according to claim 2, wherein the second metal pattern includes nickel.

5. The semiconductor package according to claim 2, further comprising:

a first insulation layer formed on a region of the upper surface of the semiconductor substrate not occupied by the plurality of chip pads; and

a second insulation layer formed on upper surfaces of the first insulation layer and the first metal pattern.

6. The semiconductor package according to claim 5, wherein the first insulation layer includes polymide or benzocyclobutene.

7. The semiconductor package according to claim 5, wherein the second insulation layer includes a photoresist layer or benzocyclobutene.

8. The semiconductor package according to claim 5, further comprising a solder mask formed on an upper surface of the second insulation layer.

9. The semiconductor package according to claim 5, wherein the external terminal includes a solder ball.

10. The semiconductor package according to claim 9, wherein the semiconductor substrate includes a wafer.

11. A method of fabricating a semiconductor package comprising the steps of:

separately forming a plurality of chip pads on an upper surface of a semiconductor substrate;

forming an irregular metal pattern electrically connected to the plurality of chip pads; and

forming an external terminal electrically connected to the metal pattern.

12. A method of fabricating a semiconductor package comprising the steps of:

separately forming a plurality of chip pads on an upper surface of a semiconductor substrate;

forming a first metal pattern on upper surfaces of the plurality of chip pads;

forming a second metal pattern having an irregular shape on an upper surface of the first metal pattern; and

forming an external terminal electrically connected to the second metal pattern.

13. The method according to claim 12, further comprising the step of forming a first insulation layer on a region of the upper surface of the semiconductor substrate not occupied by the plurality of chip pads.

14. The method according to claim 13, wherein the step of forming the second metal pattern comprises:

coating a photoresist layer on the upper surface of the first metal pattern;

forming an irregular photoresist layer pattern and a second insulation layer by patterning the photoresist layer;

forming a metal layer in a space of the irregular photoresist layer pattern; and

removing the irregular photoresist layer pattern.

15. The method according to claim 14, wherein the step of forming the metal layer in the space of the irregular photoresist layer pattern is carried out according to an electro-plating process.

16. The method according to claim 14, further comprising a step of forming a solder mask on an upper surface of the second insulation layer so that a region of the second metal pattern is exposed.

17. The method according to claim 16, wherein the step of forming the external terminal comprises the steps of:

coating a solder paste on upper surfaces of the solder mask and the second metal pattern; and

performing a reflow process on the solder paste.

18. The method according to claim 13, wherein the step of forming the second metal pattern comprises the steps of:

coating a photoresist layer on the upper surface of the first metal pattern;

forming an irregular photoresist layer pattern by patterning the photoresist layer;

forming a metal layer in a space of the irregular photoresist layer pattern;

removing all the photoresist layers including the irregular photoresist pattern;

coating a second insulation layer on the upper surface of the first metal pattern; and

patterning the second insulation layer so that the upper and side portions of the metal layer are exposed.

19. The method according to claim 18, wherein the step of forming the external terminal comprises the steps of:

coating a solder paste on upper surfaces of the second insulation layer and the second metal pattern; and

performing a reflow process on the solder paste.

20. The method according to claim 12, wherein the first metal pattern includes titanium and the second metal pattern includes nickel.

ABSTRACT OF THE DISCLOSURE

A semiconductor package and a fabrication method thereof can enhance adhesion between a solder and a package body by employing an irregular metal pattern, and improve stability. The semiconductor package includes a semiconductor substrate; a plurality of chip pads separately formed on an upper surface of the semiconductor substrate; an irregular metal pattern electrically connected to the plurality of chip pads; and an external terminal electrically connected to the metal pattern. In addition, a method of fabricating the semiconductor package includes the steps of separately forming a plurality of chip pads on an upper surface of a semiconductor substrate; forming an irregular metal pattern electrically connected to the plurality of chip pads; and forming an external terminal electrically connected to the metal pattern.

FIG. 1
BACKGROUND ART

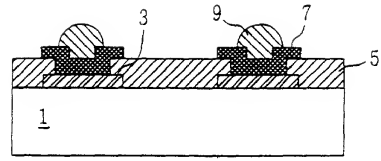


FIG. 2

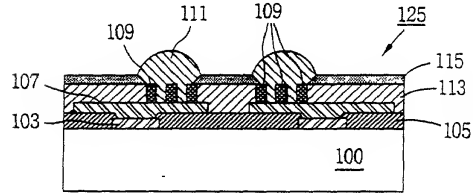


FIG. 3A

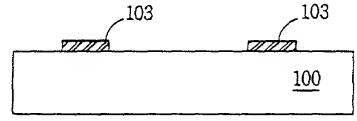


FIG. 3B

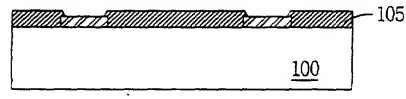


FIG. 3C

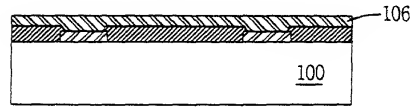


FIG. 3D

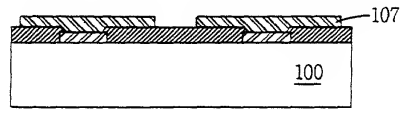


FIG. 3E

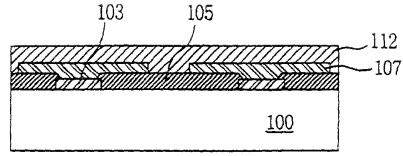


FIG. 3F

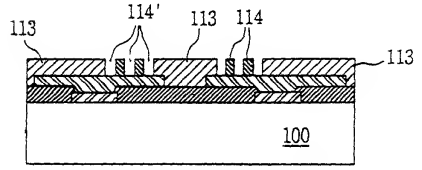


FIG. 3G

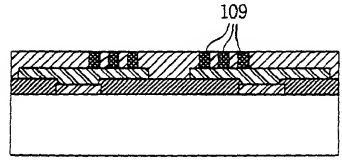


FIG. 3H

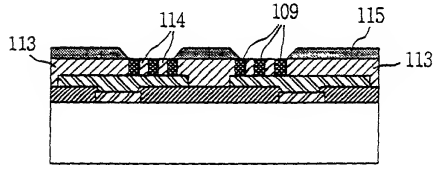


FIG. 3I

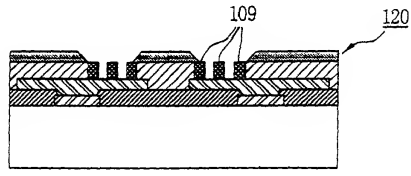


FIG. 3J

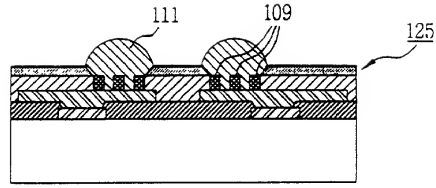


FIG. 4A

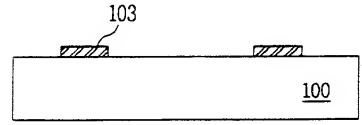


FIG. 4B

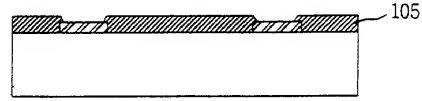


FIG. 4C

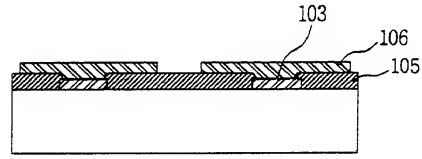


FIG. 4D

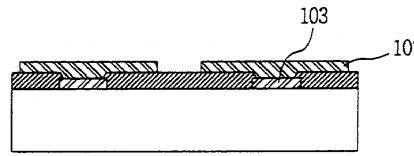


FIG. 4E

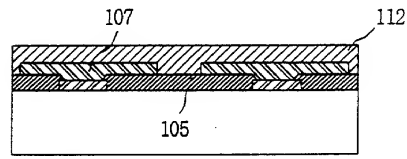


FIG. 4F

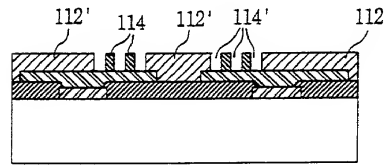


FIG. 4G

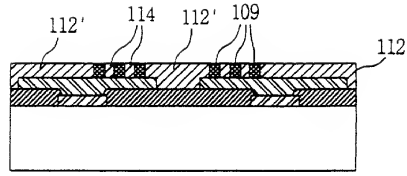


FIG. 4H

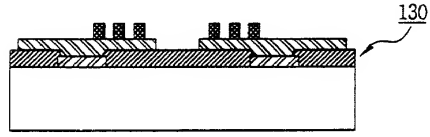


FIG. 4I

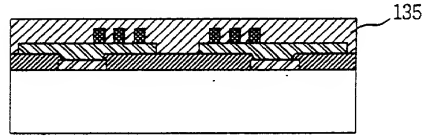


FIG. 4J

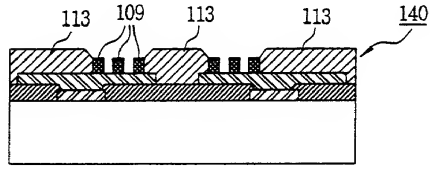
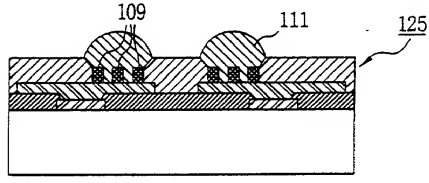


FIG. 4K



COMBINED DECLARATION FOR PATENT APPLICATION AND POWER OF ATTORNEY

U.S. DEPARTMENT OF COMMERCE
Patent and Trademark Office

ATTORNEY DOCKET NO.: 041993-5151

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR PACKAGE AND FABRICATION METHOD THEREOF

the specification of which:

is attached hereto; or

was filed as United States application Serial No. _____ on _____ and was amended on _____(if applicable); or

was filed as PCT international application Number _____ on _____ and was amended under PCT Article 19 on_____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office information which is material to the patentability of claims presented in this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119(a)-(d) or §365(b) of any foreign application(s) for patent or inventor's certificate or §365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN APPLICATION(S):

COUNTRY (if PCT, indicate PCT)	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED
KOREA	285/2000	5 January, 2000	[X] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No
			[ ] Yes [ ] No

Combined Declaration For Patent Application and Power of Attorney - **(Continued)**
(includes Reference to PCT International Applications)

ATTORNEY DOCKET NO.: 041993-5151

I hereby claim the benefits under Title 35, United States Code §119(e) of any United States provisional application(s) listed below.

U.S. PROVISIONAL APPLICATIONS

U.S. PROVISIONAL APPLICATION NO.	U.S. FILING DATE

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) or §365(c) of any PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of claims presented in this application in accordance with Title 37, Code of Federal Regulations, §1.56 which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATIONS DESIGNATING THE U.S. FOR BENEFIT:

U.S. APPLICATIONS		STATUS (Check One)		
U.S. APPLICATION NO.	U.S. FILING DATE	PATENTED	PENDING	ABANDONED

POWER OF ATTORNEY: As a named inventor, I hereby appoint the registered practitioners of Morgan, Lewis & Bockius LLP included in the Customer Number provided below to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and direct that all correspondence be addressed to that Customer Number.

Customer Number: 009629

Direct Telephone Calls To:
(name and telephone number)

Robert J. Gaybrick
202-467-7501

Combined Declaration For Patent Application and Power of Attorney - **(Continued)**
(includes Reference to PCT International Applications)

ATTORNEY DOCKET NO.: 041993-5151

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

FULL NAME OF SOLE OR FIRST INVENTOR	Seong-Kweon HA	
RESIDENCE & CITIZENSHIP	Kyoungki-Do KOREA	COUNTRY OF CITIZENSHIP Republic of Korea
POST OFFICE ADDRESS	10/6, 214-5, Yeijungbu 4-Dong, Yeijungbu, Kyoungki-Do, KOREA	
FIRST OR SOLE INVENTOR'S SIGNATURE	Seong-Kweon HA	DATE Oct. 20, 2000
FULL NAME OF SECOND INVENTOR	Jong-Hun KIM	
RESIDENCE & CITIZENSHIP	Choongcheongbuk-Do KOREA	COUNTRY OF CITIZENSHIP Republic of Korea
POST OFFICE ADDRESS	LG Employee Apt. Ka-703, Bongmyoung 2-Dong, Heungduk-Ku, Cheongju, Choongcheongbuk-Do, KOREA	
SECOND INVENTOR'S SIGNATURE	Jong Hun Kim	DATE Oct. 20, 2000
FULL NAME OF THIRD INVENTOR		
RESIDENCE & CITIZENSHIP		COUNTRY OF CITIZENSHIP
POST OFFICE ADDRESS		
THIRD INVENTOR'S SIGNATURE		DATE

Listing of Inventors Continued on attached page(s) [ ] Yes [X] No